A 76-81 GHz FMCW 2TX/3RX Radar Transceiver with Integrated Mixed-Mode PLL and Series-Fed Patch Antenna Array

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Abstract— This paper presented a 76-81 GHz FMCW MIMO Radar transceiver with mixed-mode PLL. Utilizing series-fed patch antenna array, a prototype system is developed based on the proposed transceiver. On-chip Measurements show that reconfigurable sawtooth chirps could be generated with a bandwidth up to 4 GHz and a period as short as 30 μs. Real-time experiments demonstrate that the prototype MIMO radar has the ability of target detection and achieves an angular resolution of 9°

I. Introduction

In recent years, with the development of automotive technique, the demand for high performance millimeter radar has grown rapidly. Several W-band FMCW radar transceivers have been presented [1–3]. However, these works suffer from inflexible PLL loop bandwidth and limited angular resolution. Additionally, less attention has been paid on TX-leakage and short-range interference, which may deteriorate RX performance.

In this work [4], a FMCW radar transceiver is presented by using a mixed-mode PLL with flexible loop bandwidth. 2 TX, 3 RX and cascadable LO scheme are presented for MIMO to improve angular resolution. High linearity RX is utilized to deal with TX-leakage. A prototype system is also developed with series-fed patch antenna array.

II. Proposed Radar Transceiver and Prototype

A. System Architecture

Fig. 1 shows the block diagram of the proposed FMCW radar transceiver. The system consists of a mixed-mode PLL for chirp generating, a frequency doubled LO network with input/output buffers for LO signal distribution and chip cascading. Two TXs and three RXs are integrated for MIMO operation. To resist TX-leakage, high RX linearity is achieved by utilizing a low-gain LNA, a voltage-mode passive mixer and a high-pass IF amplifier. Each TX consists of a PA with fast on/off switch and a Bi-Phase modulation stage for OOK and BPSK MIMO operation

B. Mixed-mode PLL

In the mixed-mode PLL, a digital loop filter is used to reconfigure the loop bandwidth according to different chirp waveforms. A low-mismatch wide-range 2-D Venier TDC is employed to detect the divided clock period. As shown in Fig. 2(a), a delay lock loop(DLL) is utilized to calibrated the delay mismatch between two delay chains. Assuming the unit delay time of two chain are $\tau_x = m\Delta$ and $\tau_y = (m-1)\Delta$, the DLL configures the delay unit of two chains till the delay time difference between the outputs of $(m-1)th$ stage of X and mth stage of Y equals zero. The dynamic range of the DAC is important for generating almost-ideal sawtooth FMCW chirp since the DAC's output represents the slope of the waveform. As illustrated in Fig. 2(b), a coarse-fine DAC with a 10 μA fine LSB and a 1.28 mA coarse LSB is presented, supporting a chirp slope up to 4 GHz/5 μs.

C. Series-Fed Patch Antenna Array

As shown in Fig. 3, based on the proposed FMCW radar transceiver, a two-chip cascaded 4T6R radar prototype is presented. PCB-based non-uniform excited series-fed patch antenna array is employed. The gain and side lobe level of one single antenna achieve 11.2 dB and -20 dB, respectively [4]. With a spacing of 2.2 mm, the theoretical field of view(FOV) of the antenna array achieves ±55°

III. Measurement Results

The proposed radar transceiver is fabricated in a 65nm CMOS technology with a chip area of 7.29 mm^2. Fig. 3(a) shows the chip photo. Fig. 4 depicts the measured phase noise of the PLL at 39.2 GHz carrier. Demodulated FMCW chirps with different configurations are shown in Fig. 5. Two corner reflectors placed 5 m away are used to measure the angular resolution and FOV of the prototype. As shown in Fig. 6, a 9° angular resolution and a 106° FOV are achieved. Fig. 7 illustrated the environment and result of the real-time measurement in multi-target scenario. The result shows that Flag poles, trees and bikes are correctly detected.

IV. Conclusion

This paper presents a 76-81 GHz FMCW radar transceiver with mixed-mode PLL and a PCB-based radar prototype with series-fed patch antenna array [4]. The on-chip and real-time measurements show that the presented radar system has the ability of multi-target detection and the potential of practical application.

Acknowledgements

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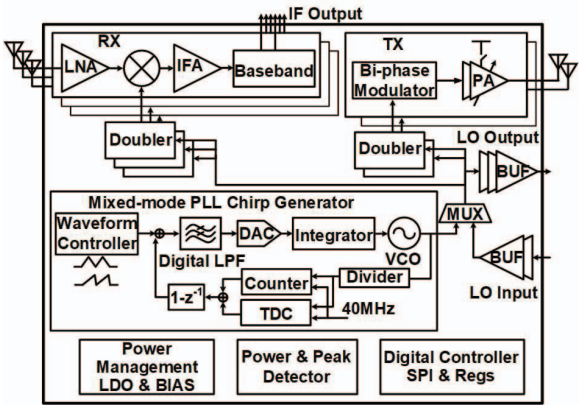
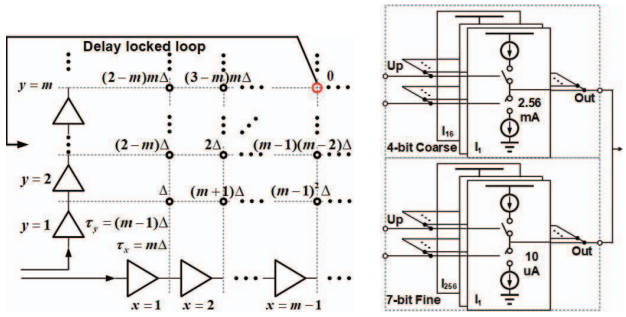
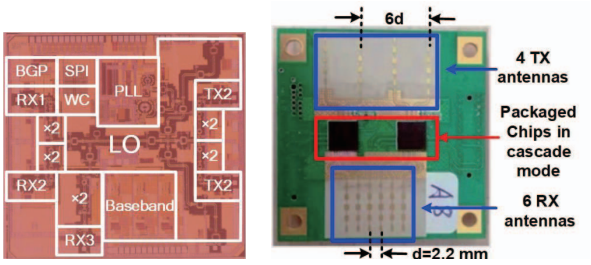


Fig. 1. System block diagram of the presented FMCW transceiver. [4]



(a) (b)

Fig. 2. (a) Conceptual block diagram of the 2-D Venier TDC and the calibration loop. (b) Schematic of the current steering DAC. [4]



(a) (b)

Fig. 3. (a) Chip Photograph (x2 = doubler, WC = Waveform Controller). (b) Photograph of the RF board including TX/RX antenna arrays and cascaded packaged chips. [4]

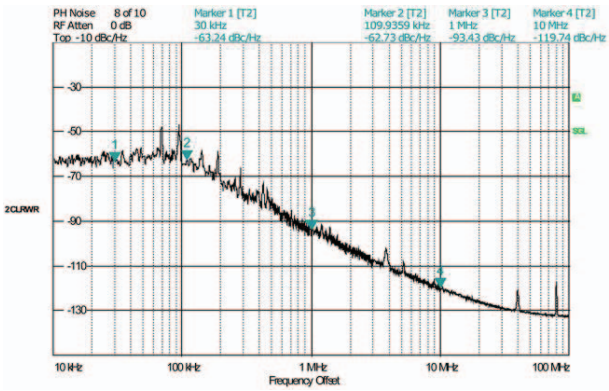
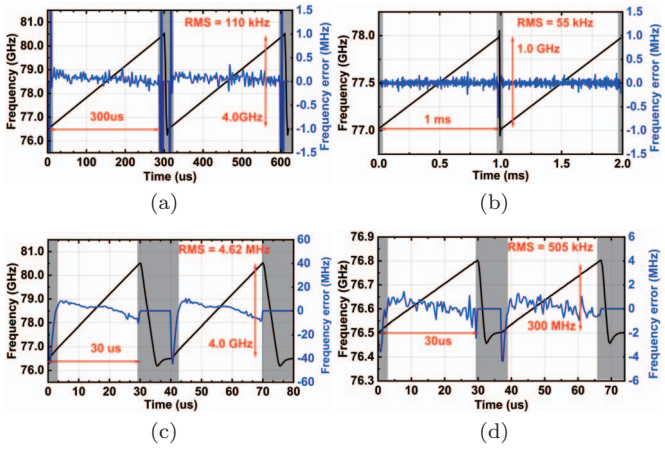
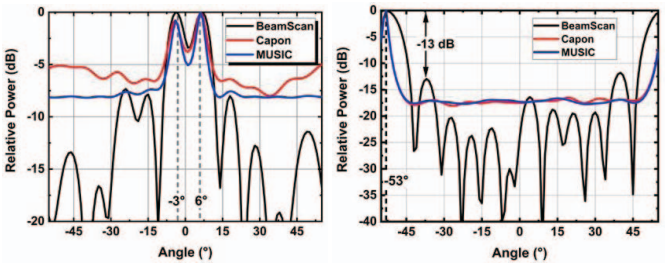


Fig. 4. Measured phase noise of the PLL locked at 39.2 GHz fixed frequency point. [4]



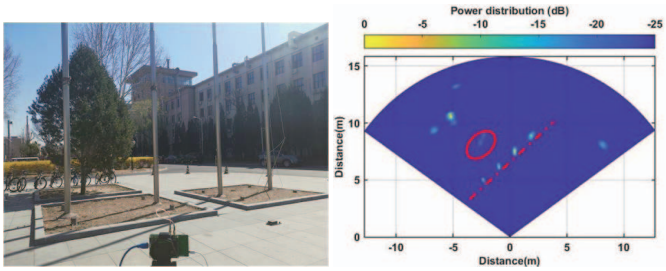
(a) (b) (c) (d)

Fig. 5. Demodulated FMCW chirps and frequency error without turning points under different configurations: (a) 300 μs & 4 GHz, (b) 1 ms & 1 GHz, (c) 30 μs & 4 GHz, (d) 30 μs & 300 MHz. [4]



(a) (b)

Fig. 6. (a) Measured angle pattern with two corner reflectors. (b) Measured FOV. [4]



(a) (b)

Fig. 7. (a) Multi-target measurement scenario. (b) Measured 2-D normalized power distribution of multi-target scenario. [4]

TABLE I
PERFORMANCE COMPARISON

	[1]	[2]	[3]	This Work
Process	65nm CMOS	65nm CMOS	45nm CMOS	65nm CMOS
Channel	1T1R	1T2R	3T4R	2T3R
Chirp BW (GHz)	0.7	1.93	4	4
Chirp Slope (MHz/us)	1.4	1.93	100	13.3/133[a]
RMS error (kHz)	65	674	-	110/4620[a]
Phase noise (dBc/Hz)	-85.53	-81	-94	-87
Area/channel[b] (mm^2)	1.04	2.32	1.83	1.22
Power/channel[b] W	0.243	0.172	0.283	0.154

[a]The RMS frequency error of 4 GHz/300 μs and 4 GHz/30 μs sawtooth chirp are 110 kHz and 4.62 MHz, respectively.

[b]The average area and consumption of the formed each MIMO virtual channel (N RX + M TX means N*M virtual channels).