A *Ka*-Band 4TX/4RX Dual-Stream Joint Radar-Communication Phased-Array CMOS Transceiver

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***Abstract*— A *Ka*-band 4TX/4RX dual-stream joint radar-communication phased-array transceiver is presented for the emerging radar-communication integrated wireless system. Different from the existing joint radar-communication transceiver with separated downconversion path and analog baseband, the proposed joint radar-communication transceiver features completely reused hardware components. In addition, various circuit design challenges in the joint radar-communication transceiver are addressed. In order to enhance the signal-to-noise and distortion ratio (SNDR) in low input power region for the communication mode and effectively reduce the chip area, a current-flopping bidirectional active mixer is proposed. A variable-transmission-line-based phase shifter (TL-PS) with tiling structure is introduced to achieve wideband phase shifting with flat group delay and in-band loss fluctuation. A pseudo-stacked power amplifier (PA) is introduced to provide both high linearity and high saturated output power for the joint radar-communication transceiver. A 4TX/4RX dual-stream joint transceiver is designed and fabricated in a standard 65-nm complementary metal–oxide–semiconductor (CMOS) process with the chip area of 16.2 mm^2. The measured results show that the TRX covers 28.7–36.2 GHz with the peak gain of 22.2/34.7 dB for TX/RX. The measured TX peak saturated output power is 19.9 dBm and the $OP_{1\ dB}$ is 17.4 dBm. The measured RX minimum noise figure (NF) is 4.8 dB and the $IP_{1\ dB}$ is > -31.5 dBm. In addition, the analog baseband offers a 3.5-GHz bandwidth for the wideband radar signal. System measurement indicates that the proposed transceiver supports real-time centimeter-level 2-D imaging and 400-Msym/s 64-quadrature amplitude modulation (QAM) over-the-air (OTA) wireless link.**

***Index Terms*— Bidirectional mixer, communication, joint radar communication, phased array, radar sensing.**

I. Introduction

RECENT years have witnessed a growing research interest in the study of joint radar-communication wireless systems. Such kind of integrated multifunctional wireless systems show significant advantages in terms of spectrum efficiency, compact size, performance co-optimization, energy efficiency, and the overall cost compared to the assembling of two distinct systems [1], [2], [3], [4], [5], [6], [7]. Emerging applications that require joint sensing and communication include vehicle-to-vehicle (V2V) communication scenarios [8], [9], [10], environment monitoring [11], future mobile networks [12], [13], [14], the Internet of Things [15], and so on. For example, unmanned aerial vehicle (UAV) is considered as a critical component for future cellular networks, as shown in Fig. 1, which necessities both remote sensing function for localizing targets/sensing environments and instant communication function simultaneously [16], [17], [18]. Integrated in a unified platform with cooperative coexistence, the two functions are allowed to access the same spectrum and employ a shared antenna array, which contributes to reduce the scale of RF elements [19], [20]. Furthermore, under various application scenarios, the transceiver beam streams are desired to be allocated dynamically between radio communication and radar sensing mode depending on the requirements/conditions on user numbers, instantaneous data throughput, and surrounding environments, which leads to better overall system utilization.

The recent literature on joint radar/communication system is increasingly extensive. However, most related research advances focus on the structure modeling and signal processing algorithms [12], [21], [22], [23]. In this article, the main purpose is to investigate the feasibility of joint radar-communication transceivers from the viewpoint of integrated circuits and wireless systems.

Along with the scaling of complementary metal–oxide–semiconductor (CMOS) technology, designing millimeter-

Manuscript received 17 May 2023; revised 29 July 2023; accepted 31 August 2023. Date of publication 26 September 2023; date of current version 6 March 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 62131013, in part by the Shenzhen Science and Technology Program under Grant JCYJ20200109113601723 and Grant JCYJ20210324115610028, in part by the Tsinghua-Samsung Joint Research Project, in part by the Chinese Academy of Sciences (CAS) Pioneer Hundred Talents Program, and in part by the Beijing Advanced Innovation Center for Integrated Circuits. *(Corresponding author: Wei Deng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2023.3315792.

Digital Object Identifier 10.1109/TMTT.2023.3315792

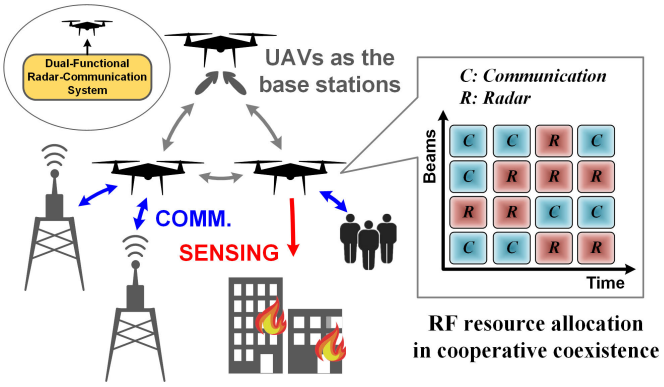


Fig. 1. UAVs with radar-communication functions take on the role of air-base station in fire rescue.

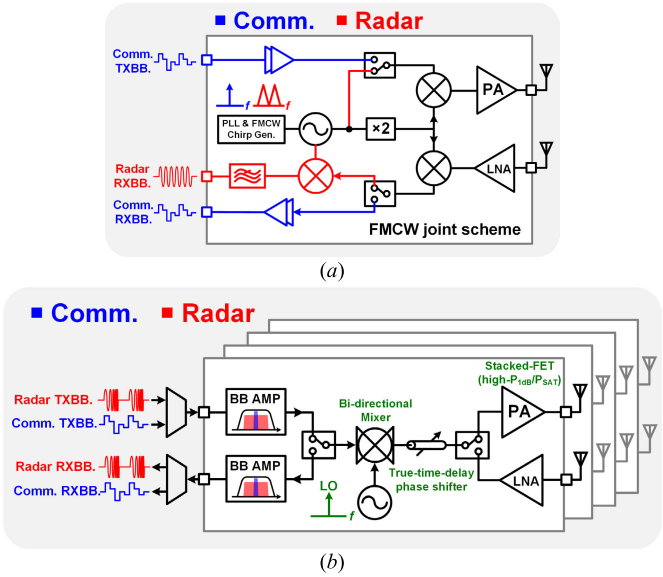


Fig. 2. Simplified block diagram of (a) conventional joint radar-communication transceiver structure using FMCW scheme and (b) proposed joint radar-communication transceiver structure using pulsed chirp scheme.

wave (mm-wave) wireless transceivers using bulk CMOS technology becomes feasible. Several mm-wave CMOS transceivers dedicated to either wireless communication [24], [25], [26], [27], [28], [29], [30], [31], [32] or radar sensing [33], [34], [35] applications have been successfully demonstrated during the past few years. However, there are few silicon-based mm-wave transceivers with joint radar-communication function reported so far. In an existing case [36], [37], a *D*-band 1TX/1RX dual-mode transceiver supporting frequency-modulated continuous-wave (FMCW) radar and wireless communication function is introduced [see Fig. 2(a)]. However, power-switching-based mode multiplexers are inevitably required for performing switching between either the radar mode or the communication mode. Therefore, the reported joint-radar-communication transceiver can operate in a time-division manner only. In addition, given that there is a significant difference in the signal bandwidth and linearity requirement for the communication and the FMCW radar mode, the analog baseband (BB) and the downconversion path have to be designed separately, which leads to incomplete hardware reusage. Third, beamforming technique has great potential for the joint radar-communication system. Although beamforming has been intensively studied for wireless communication and radar sensing, it is not straightforward to directly apply beamforming to the joint radar-communication transceiver as there are different circuit and system requirements, for example, instantaneous signal bandwidth for wireless communication and radar sensing. Mannem et al. [38] proposed an upmixing joint radar-communication transmitter with frequency modulation for sensing-aided communication, and it can likewise be operated as a radar for sensing. Nevertheless, its sensing function is mainly used for angular localization of RX nodes and targets in azimuth rather than range measurement. In addition, the radar mode is discussed based on narrowband intermediate frequency (IF)/BB signals with limited potential range resolution. Up until now, there has been no silicon-based phased-array joint radar-communication transceiver with both uplink and downlink reported so far.

In order to overcome the abovementioned issues, this article investigates the possibility and feasibility of a firmly integrated joint-radar-communication transceiver with sharing (almost all) hardware components. Different from using FMCW scheme as radar sensing in the existing joint-radar-communication transceiver, pulsed chirping scheme [see Fig. 2(b)] is adopted in the radar mode of the joint-radar-communication transceiver. The pulsed chirping scheme in the radar mode features direct upconversion/downconversion by I/Q mixers, which is completely compatible with quadrature modulation-based communication scheme. On the other hand, pulsed chirp scheme enables time division for uplink and downlink, which is identical to the communication operation mode. Therefore, it is possible to achieve a fully reused joint-radar-communication transceiver from architecture view of point potential for the joint radar-communication system. In order to support the simultaneous operation of both radar and communication, a multibeam joint radar-communication transceiver is introduced for generating beamforming waveform with two or more streams for communication and sensing, respectively. Each stream could work with the dual function in time or frequency division. Furthermore, the streams can be controlled separately for radar sensing or radio communication and present several combinations such as two independent radar streams, two independent communication streams, or one radar stream together with one communication stream. This enables the transceiver system to realize dynamic resource allocation for various application scenarios.

In this article, a *Ka*-band 4TX/4RX dual-stream phased-array joint radar-communication transceiver is presented. A 2-D measurement in the radar mode and 64-quadrature amplitude modulation (QAM) wireless communication over-the-air (OTA) link is successfully demonstrated. In addition, various circuit design challenges in the joint radar-communication transceiver are addressed. A current-flipping bidirectional active mixer is proposed to enhance the system signal-to-noise and distortion ratio (SNDR) in the low P_{in} region (communication mode and linear power region) and reduce the chip area. A pseudo-stacked power amplifier (PA) is presented and compatible for both high gain and output power. In addition, a variable-transmission-line-based phase shifter (TL-PS)

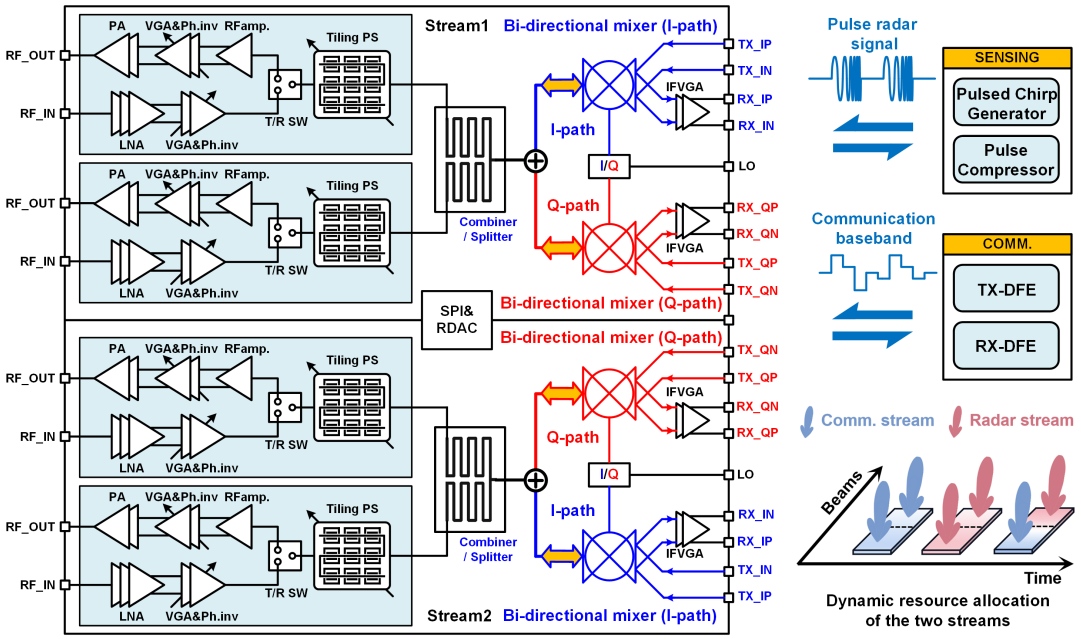


Fig. 3. Top-level diagram of the proposed four-channel phased-array transceiver.

with tiling topology is introduced to achieve wideband phase shifting and mitigate the in-band loss fluctuation.

Implemented in a 65-nm CMOS technology, the transceiver covers a 28.7–36.2-GHz frequency range. The measured TX output 1-dB compression point is 17.4 dBm and the measured RX minimum noise figure (NF) is 4.8 dB. A completely functional 400-Msym/s 64-QAM OTA wireless link and a centimeter-level 2-D imaging system prototype are demonstrated with the measured system performance.

This article is the extended version of [39] and is organized as follows. Section II discusses the overall architecture of the proposed transceiver with fusion design considerations and explanation of pulsed chirp radar principle. Section III presents the transceiver building block design. Section IV demonstrates the experimental results of the transceiver. Finally, the conclusion is presented in Section V.

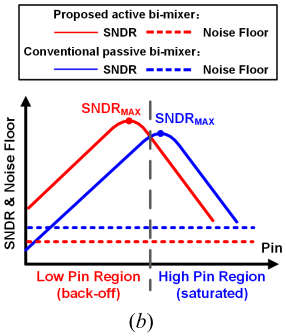
II. Transceiver Architecture and Pulsed Chirp Principle

A. Transceiver Architecture

The detailed block diagram of the proposed four-channel dual-stream joint radar-communication CMOS transceiver is shown in Fig. 3. Every two channels support an individual stream and are converged by a passive combiner/splitter and connects to a pair of I/Q mixers. The proposed active I/Q mixers are bidirectional and work for both the uplink and the downlink. It reduces the number of mixers by half in the whole chip, with only cost of a T/R switch required to toggle the TX or RX front end. The T/R front end consists of a stacked-field-effect transistor (FET) PA, a three-stage low-noise amplifier (LNA), a current-mode variable-gain amplifier (VGA), and an RF buffer. There is no passive attenuator in the receive/transmit chain to avoid undesired insert loss. A TL-PS is reused by the TX and RX to provide phase control for beamforming, and it adopts the true-time-delay-like topology

The gain budgets of the proposed TX circuits					
TX	Mixer	Passive	RFAMP.	VGA+PA	Total
Gain/dB	−8	−19	10	36	-
Cumulative Gain/dB	−8	−27	−17	19	19

(*a*)



(*b*)

The link budgets of the proposed RX circuits					
RX	LNA+VGA	Passive	Mixer	IF amp.	Total
Gain/dB	35	−19	−6	17	-
Cumulative Gain/dB	35	16	10	27	27
NF/dB	5.0	19	7.5	15	-
Cascade NF/dB	5.0	5.1	5.2	8.1	8.1
OIP3/dB	17.8	20	2.4	12	-
Cumulative OIP3/dB	17.8	−1.2	−7.6	7.5	7.5
Noise Floor = −52.8dBm			SNDR$_{MAX}$ = 31.8dB		

(*c*)

Fig. 4. Link simulation of the transceiver. (a) Link budgets of the proposed TX circuits. (b) SNDR and noise floor with a passive or an active mixer. (c) Link budgets of the RX.

to achieve the wideband characteristics for the radar mode. The baseband I/O ports are shared for both data stream in the communication mode and pulsed chirp signals in the radar mode. A baseband VGA following each mixer, only for the RX chain, compensates the loss of the mixer and expands the baseband bandwidth.

It is clear that the bidirectional mixer shared by the TX and the RX contributes to simplifying the local oscillator (LO)/baseband distribution network and reduces the chip area considerably. Besides, it is crucial to ensure a higher sensing and communication quality, compared to passive mixers. While typical passive mixers are inherently bidirectional, their low conversion gain leads to deteriorated system performance in terms of link gain, SNDR, and noise floor for a

phased-array transceiver, as shown in Fig. 4. First, the power gain in the TX chain is important due to the considerable undesired power loss from the phase shifter, gain controller, and path switches in a phased-array beamformer. Moreover, the radar operation requires signals transmitted in the saturated region, and the gain of the TX link should be maximized. Fig. 4(a) shows the TX gain budget. For the TX link, using a passive mixer will reduce the conversion power gain obviously. Thus, the reduced link gain due to lossy passive mixers needs to be compensated by other power-hungry circuits, including the PA, RF VGA, and RF buffers. Apparently, this will lead to extra dc power and cancel out the advantage of using a zero-consumption passive mixer. Therefore, an active mixer is preferred to the TX mode by comparison. Second, for RX, the error vector magnitude (EVM) of the received signal in the communication mode is directly affected by SNDR, as expressed in the following:

$$\mathrm{SNDR} = \frac{P_{\mathrm{in}} \cdot G_{\mathrm{T/R}}}{\mathrm{IM}_3 + \mathrm{KT} \cdot B \cdot G_{\mathrm{T/R}} \cdot \mathrm{NF}} \tag{1}$$

where P_{in} is the input signal power, $G_{\mathrm{T/R}}$ is the link gain, IM_3 is the third intermodulation product, $\mathrm{KT} \cdot B$ is the input noise power, and NF is the noise figure. As shown in Fig. 4(b), an active mixer has a better SNDR in the linear region with a lower noise floor than a passive mixer. Considering that the transceiver in the communication mode is operated in the linear region and the radar operation is not sensitive to amplitude distortion, the active bimixer is obviously introduced as a more competent solution here. Fig. 4(c) summarizes the RX link budget of the proposed transceiver. While the LNA and VGA provide 37-dB power gain in total, the passive modules provide a 19-dB power loss. The active bimixer has a −6-dB conversion gain, followed by the baseband amplifier with a 17-dB gain. Compared with a passive mixer of the same size, the gain of the proposed active mixer is 5 dB higher, the noise is 0.5 dB higher, and the OIP3 is 2.6 dB lower (the comparison between active and passive mixers is performed with the same size of Gilbert transistors, i.e., 32 × 1 μm/60 nm). Thus, it can be seen that an RX using the proposed active mixer shows 3.1-dB lower noise floor and 2.2-dB higher peak SNDR, which leads to better system link performance.

B. Pulsed Chirp Radar Principle

In this work, the pulsed chirp radar scheme is adopted since it is completely compatible with quadrature modulation-based communication scheme and enables time division for uplink and downlink. In each pulse period, the frequency of the carrier is linearly modulated, as shown in Fig. 5. The functions of 1-D ranging and 2-D imaging are demonstrated in this work, and the operation principle of the pulsed chirp radar sensing is introduced in the following.

Unlike narrow or spike pulse, the linear frequency-modulated (LFM) pulse signal features broad bandwidth as well as large time width. Hence, it has the merits of high average transmitted power, moderate peak-to-average power ratio (PAPR), and decent resolution [40]. For the 1-D ranging scenario, after the pulse signal is emitted from the TX, the RX converts the received RF echo to baseband and delivers it

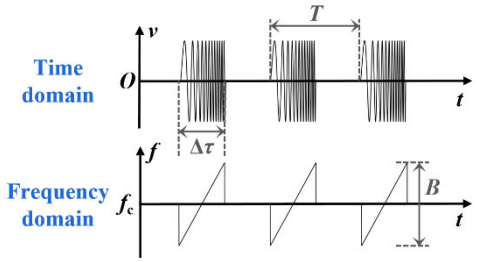


Fig. 5. Waveform and frequency modulation of pulsed chirp in time domain.

to digital processing modules. Pulse compression technique is utilized to enable the resolvability of the baseband signal by matched filtering [41]. With the TX baseband signal indicated by $p(t)$, the transmitted radar signal s_{TX} is expressed in (2), where f_c is the carrier frequency. After coherent mixing, the baseband signal s_{RX} in time and frequency domains is given in (3) and (4), respectively, where i is the order of the scatter, A_i and R_i are the amplitude and range of the scatter i, respectively, c is the light velocity, and $S(f)$ is the spectrum of $s(t)$

$$s_{\mathrm{TX}} = s(t)e^{2\pi f_c t} \tag{2}$$

$$s_{\mathrm{RX}} = \sum_i A_i s\left(t - \frac{2R_i}{c}\right) e^{-j\frac{4\pi f_c R_i}{c}} \tag{3}$$

$$S_{\mathrm{RX}}(f) = \sum_i A_i S(f) \cdot e^{-j\frac{4\pi(f_c+f)R_i}{c}}. \tag{4}$$

Matched filtering means multiplying by the conjugate function of the $S(f)$, and the pulse compression result s_{PC} is obtained in (5a)

$$\begin{aligned} s_{\mathrm{PC}}(t) &= F_{(f)}^{-1}\left[S_{\mathrm{RX}}(f)S^*(f)\right] \\ &= F_{(f)}^{-1}\left[\sum_i A_i S(f)S^*(f)e^{-j\frac{2\pi(f_c+f)R_i}{c}}\right] \\ &= \sum_i A_i e^{-j\frac{2\pi f_c R_i}{c}} \mathrm{psf}\left(t - \frac{2R_i}{c}\right) \end{aligned} \tag{5a}$$

$$\mathrm{psf}(t) = F_f^{-1}\left[|S(f)|^2\right]. \tag{5b}$$

The waveform of function $\mathrm{psf}(t)$ is a narrow pulse with a compressed main lobe time width of $1/B$ (here, B is the signal bandwidth), which is apparently reduced from that of the original pulsed chirp [40], [42]. The position of the s_{PC} pulse in the time axis represents the range of the object, and the narrow time width is more easily distinguishable. For multiscatterers, the high-resolution range profile is able to be plotted after pulse compression, and the distance between different scatters can only be calculated when their main lobes are not overlapped. Therefore, the time resolution is a main lobe width $1/B$, and the corresponding range resolution is $c/2B$, as shown in the following:

$$\Delta R = \frac{c}{2 \cdot B}. \tag{6}$$

For 2-D imaging verification, inverse synthetic aperture radar (ISAR) imaging based on rotation model [43] is presented, as shown in Fig. 6. In the measurement, the object is on a revolving stage with a fixed angular velocity. During the

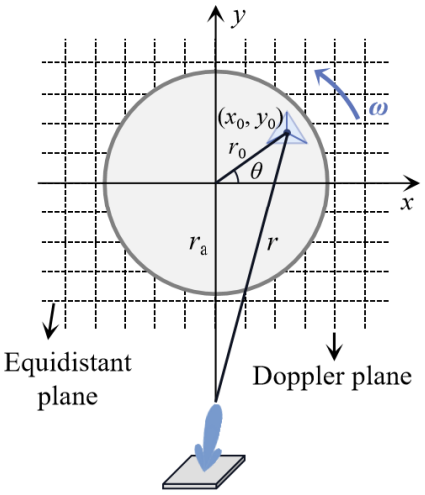


Fig. 6. Rotation model of ISAR imaging.

rotation of the object, the instantaneous distance $r(t)$ between the radar and the scatter P is expressed in the following:

$$r = \left[r_P^2 + r_O^2 + 2r_p r_O \sin\left(\theta_p + \omega t\right)\right]^{1/2} \tag{7}$$

where r_P is the range of P from O, r_O is the range of the radar from O, θ_P is the initial phase of P, and ω is the angular velocity of the stage. When $r_O \gg r_P$, (7) is converted to (8). The phase shift Φ of the reflected signal is given in (9)

$$\begin{cases} r = r_O + x_p \sin(\omega t) + y_p \sin(\omega t) \\ x_p = r_p \cos\theta_p \\ y_p = r_p \sin\theta_p \end{cases} \tag{8}$$

$$\Phi = -\frac{4\pi f_c}{c} r(t). \tag{9}$$

The scatter of the object is in motion relative to the radar system, and thus, the Doppler effect is apparent for the echo radar signal, given in (10). Because the rotation angle is generally very limited, (10) can be simplified to (11), which indicates that the Doppler frequency shift is correlated to the azimuth (i.e., the cross range of the scatter)

$$f_d = \frac{1}{2\pi}\frac{d\Phi}{dt} = \frac{2}{\lambda}\frac{dr}{dt} = \frac{2x_p\omega\cos(\omega t)}{\lambda} - \frac{2y_p\omega\sin(\omega t)}{\lambda} \tag{10}$$

$$f_d \approx \frac{2x_p\omega}{\lambda}. \tag{11}$$

Consequently, azimuth can be calculated by analyzing the Doppler frequency of the radar signal, and combining with the range measure, the 2-D coordinate of the scatter is figured out. The azimuth resolution depends on coherent accumulation time T (time of the duration of radar radiation) and is expressed as follows:

$$\Delta A = \frac{\lambda}{2\omega T} = \frac{\lambda}{2\omega N \frac{1}{\mathrm{PRF}}} \tag{12}$$

where N is the number of pulses and PRF is the pulse repetition frequency. In fact, the range-Doppler imaging algorithm is adopted to analyze the pulsed chirp echo signal. The echo signal is considered as a function of two time variables: the fast time domain (delay of the echoes from different scatters reflecting the same incident signal) and the slow time domain (the time of each pulse transmission). By applying pulse compression in the fast time domain, the range information of scatters is acquired. Then, the Doppler frequency spectrum is also drawn by the Fourier transform in the slow time domain, and subsequently, the azimuth values of scatters are obtained.

III. Circuit Design

Several circuit design challenges in the joint radar-communication phased-array transceiver are addressed. First, the active bimixer is proposed to ensure sufficient link gain and signal quality, with the reduction of the core area. Second, the true-time-delay PS provides wideband phase control for beamforming and decent in-band flatness of group delay for wideband pulsed radar signals. Third, a two-stage stacked PA with high output power and linearity is introduced for both the communication mode in the back-off state and the radar mode in the saturated region. In addition, the baseband VGA is able to expand the bandwidth of the RX baseband interface for high radar resolution, and passive attenuator is not presented for reducing link loss. In this section, the circuit implementations of the bimixer, PS, and PA are discussed in detail, and the RF VGA and baseband buffer are discussed briefly.

A. Active Bidirectional Mixer

Bidirectional mixers are desired since they can reduce the silicon area and routing complexity as well as parasitic effect at the RF ports and LO ports. Generally, conventional bimixers are passive components. However, they suffer from lower conversion gain, which deteriorates the signal strength and the RX cascaded NF, as mentioned before. Meanwhile, conventional active mixers are not able to provide reverse conversion, and thus, few related works are reported. An existing active bimixer is proposed in [44], which drives the Gilbert transistors in the saturation region and triode region in TX and RX modes, respectively, to implement the bidirectional function. However, the mixer is operated as the common-drain configuration for the RX mode, which leads to lower conversion gain than that of the TX mode. Another active bimixer is implemented in [45], and it has the same issue that the common-drain configuration is employed for the RX.

In this article, a current-flipping bidirectional active mixer is proposed by utilizing the bidirectional feature of MOS transistors. It introduces the second-order nonlinearity transconductance to enhance the conversion gain, contrary to passive designs that conduct conversion relying on the nonlinear performance of switches. Fig. 7 shows a single path model with Gilbert quad transistors of the proposed I/Q mixer, in order to analyze the bidirectional conversion. For the RX mode, the RF signal is coupled to the sources of M_1–M_4 through a transformer, whose tap is connected to a current source, with the LO fed to the gates. The drains, which are connected to the resistance loads and biased to voltage drain-to-drain (VDD), finally output the BB signal, while for the TX mode, the switches at both ends of the circuit toggle the drains to ground (GND) and the sources to VDD, with

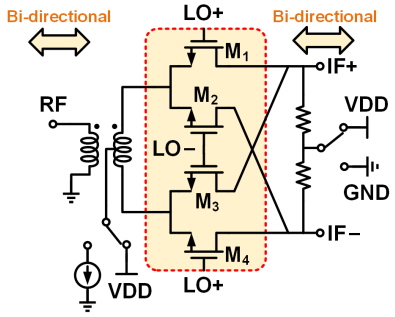


Fig. 7. Single path Gilbert quad model of the proposed bimixer.

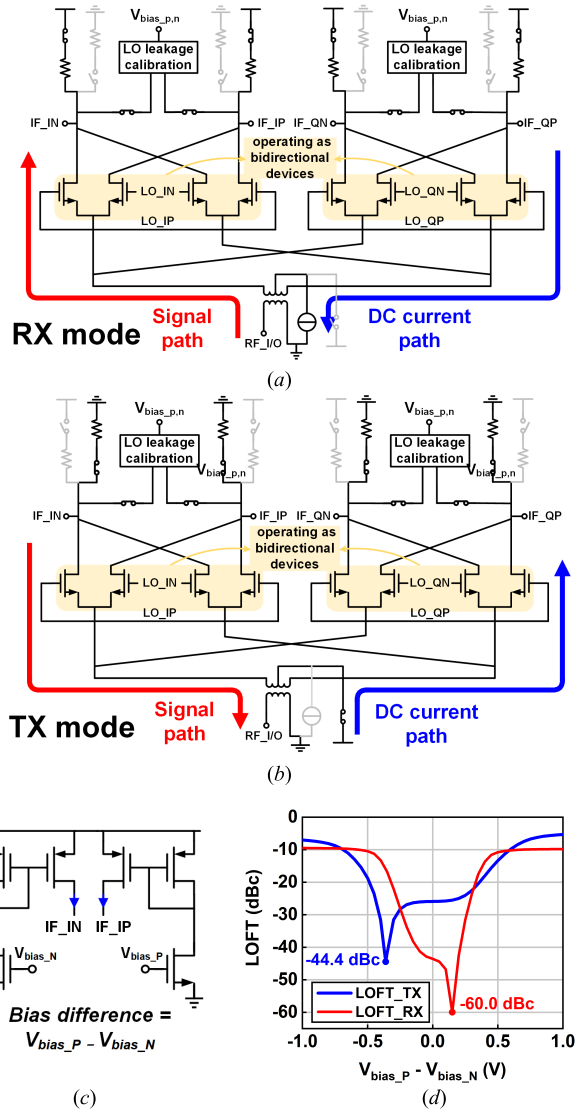


Fig. 8. Schematic and operation principle of the bimixer. (a) RX mode. (b) TX mode. (c) LOFT calibration block. (d) LOFT versus the dc bias difference.

the feed terminals of the signals remaining the same. Therefore, regardless of TX or RX, the Gilbert quad is always in a common-gate (CG) state to avoid the deterioration of the conversion gain. With appropriate gate bias, the transistors can operate in the saturation region for both TX/RX modes.

The circuit schematic of the proposed mixer and the operation principle are shown in detail in Fig. 8. This mixer has two paths for in-phase and quadrature signals and converges

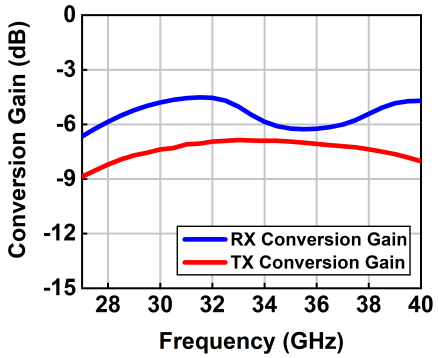


Fig. 9. Simulated conversion gain of the bidirectional mixer in the TX/RX mode.

them at the RF port. In the RX mode, the dc current flows from top to bottom, and the signal travels from bottom to top. In the TX mode, the direction states are opposite. At the BB side, a pair of switched resistors are placed at drain of each Gilbert transistor as the load or source impedance to provide dc voltage gain for satisfying the zero-IF architecture transceiver. In addition, an LO feed-through (LOFT) calibration block is introduced at this side and it is composed of a pair of pMOS current sources [see Fig. 8(c)], which inject currents to the differential nodes. In the RX mode, the injection currents are tuned to directly reduce the dc offset and the LO leakage. In the TX mode, by tuning the calibration block and the LO biases (the biases of the differential LO signals can be separately tuned, e.g., LO_IP has a different bias from LO_IN), the currents of the RF side can be varied indirectly, and hence, the LO leakage is mitigated. Fig. 8(d) plots the postlayout simulated mixer LOFT rejection versus the dc bias difference between the differential calibration current sources. The postlayout simulated results show that the calibration block can provide an LOFT rejection of −39.1/−50.4 dBc for the TX/RX mode. Fig. 9 shows the simulated conversion gain of the bimixer for both the uplink and the downlink. The in-band RF conversion gain of the TX/RX modes is better than −8/−6.5 dB, respectively.

The complete upconversion/downconversion link is shown in Fig. 10. It consists of the LO chain, I/Q mixer, and RX baseband amplifiers. The off-chip LO signal is orthogonalized by a passive polyphase filter (PPF) and then driven by a pair of PPF buffers before delivering to the mixer. The gate biases of both the PPF buffers and mixers are assigned to the I-path and Q-path separately and tuned by the resistor-based digital-to-analog converters (R-DACs) for the image rejection. Combined with the 3-bit switched resistor in the PPF, these adjustable biases can reduce the amplitude mismatch and phase mismatch during the I/Q conversion to improve the image rejection and lead to a better EVM for high-order QAM communication [46], [47]. The baseband buffer is used to compensate the gain loss and noise deterioration from the downconversion, and the bandwidth expansion method is introduced to enhance broadband fan-out ability.

B. Transmission-Line-Based Phase Shifter (TL-PS)

For high-resolution sensing, a wide instantaneous bandwidth radar signal is required. However, the conventional PSs,

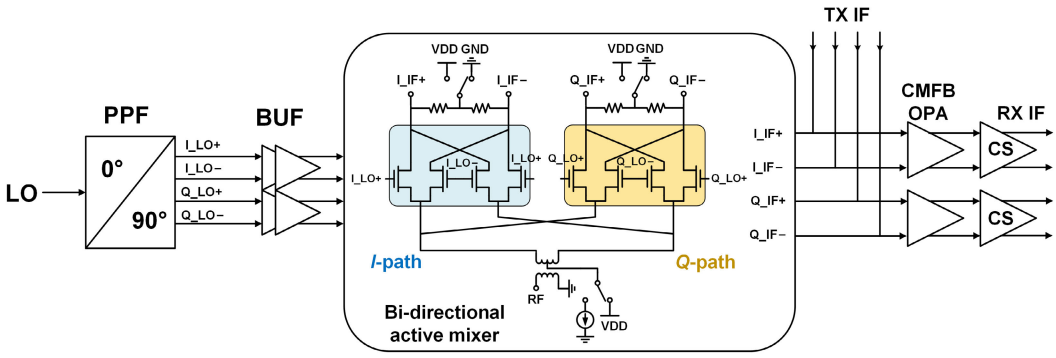


Fig. 10. I/Q conversion link.

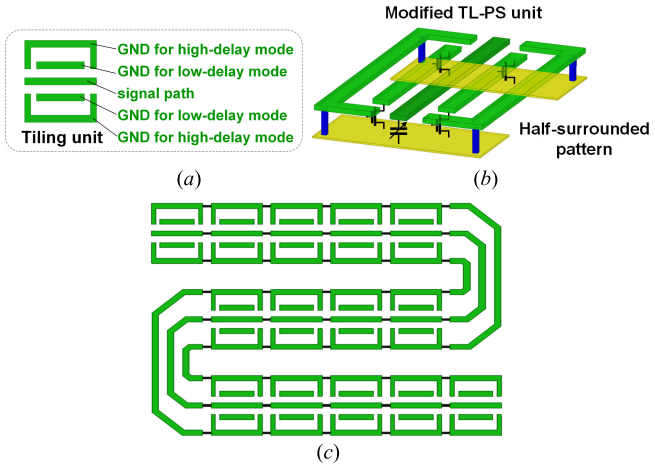


Fig. 11. Structure of the TL-PS. (a) Delay cell. (b) 3-D perspective of the delay cell. (c) Whole layout of the PS.

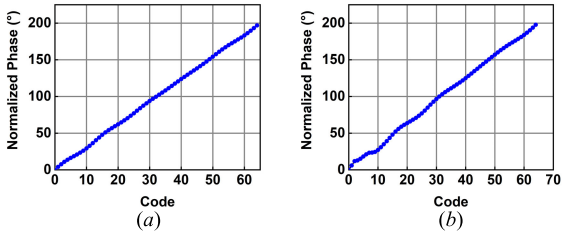


Fig. 12. Simulated normalized phase curves of two different PSs. (a) Proposed PS. (b) TL-PS with conventional delay cells.

including the reflection type, the switched LC type, and the vector modulator-based type, only exhibit narrow instantaneous bandwidth. When transmitting wideband signals, they will cause delay variation over the spectrum. To overcome group delay distortion, a true-time-delay PS is employed due to its inherent constant group delay across frequency for a wide signal bandwidth. A wideband time-delay circuit is simply implemented by a continuous transmission line, with the constant propagation delay $t_d = l\cdot(LC)^{1/2}$, where l is the length of the line and L and C are the inductance and capacitance per unit length, respectively. It is indicated that the delay time depends on the impedance characteristic of the delay line.

In this article, an S-shape tiling structure TL-PS is proposed. It consists of a series of delay unit cells with discontinuous ground line. The total delay of the proposed PS chain is proportional to the number of tiles. As a result, the design of the PS is modularized and scalable [48]. Each delay cell is composed of five lines: a signal line, two inside GND lines for low delay mode, and two outside GND lines for high delay mode, as shown in Fig. 11(a). As seen in the 3-D perspective of the delay cell [see Fig. 11(b)], in high delay mode, the inside GND lines are floated, and the outside GND lines are active, leading to increased equivalent inductance. For maintaining the characteristic impedance, a switched capacitor beneath the signal line is turned on. As a result of larger L and C, the signal line presents a high delay time. In low delay mode, the inner GND lines are connected to the ground by switches, with the switched capacitor off. The path loss of the low delay mode is less than that of the high delay mode, in order to flatten the loss difference between the delay modes, an nMOS switched resistance is added parallel to the signal line and turned on in low delay. As described previously, phase control can be realized by changing the numbers of cells in low delay and high delay. Compared to the previously reported TL-PS [49], the proposed PS uses half-surrounded GND lines (the inner GND lines are discontinuous and surrounded by the outer GND lines whose ends return to the center line in each unit), and the delay cell is reciprocal for forward and reverse propagation. As a result, the PS chain features a tiling structure with a better cascade linearity of phase shifting, according to the electromagnetic (EM) simulation results. Fig. 12 shows the simulated normalized phase of the proposed PS and a TL-PS with conventional delay cells. It can be seen that the former has a slight phase fluctuation compared to the latter. The integral nonlinearity (INL) errors with control code are also plotted in Fig. 13. The error variation range of the proposed PS is much smaller, with a better peak value (2.1°), than that of the referenced TL-PS (5.2°). Fig. 11(c) shows the complete layout of the PS, with the width of the signal line and the GND lines of 8 μm. Due to the bending tiles, the PS is constructed into an S-shape, to limit the length of the chain and optimize the top-level floorplan of the transceiver.

The proposed TL-PS can provide 6-bit phase control aimed to cover 180° shifting. A binary-to-thermometer decoder is adopted to convert the control words to toggle the state of each delay cell. Based on the simulation, the PS realizes a phase resolution of less than 3.5° and exhibits a limited spectrum loss fluctuation of 4 dB within the whole *Ka*-band, with an added

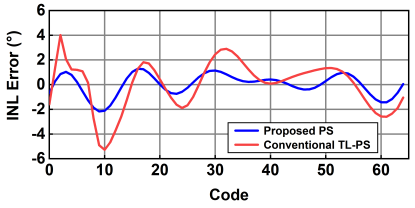


Fig. 13. Simulated INL phase error of the proposed PS and the referenced PS.

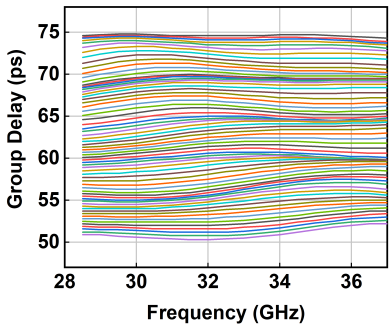


Fig. 14. Simulated group delay with different phase levels of the proposed PS.

amplitude modulation of less than 1 dB for phase shifting. For wideband radar signal, the proposed PS presents an appropriate group delay performance. The simulated ripple of the group delay at every delay state is <2.7 ps across the band, i.e., 8% of a period of a 30-GHz signal, as shown in Fig. 14.

C. Pseudo-Stacked PA

The PA with both high linearity and high output power is desired for the joint radar-communication transceiver. Under a double or triple regular supply voltage, a conventional standard stacked PA can offer a relatively high output impedance, which causes a low impedance conversion ratio for output matching from 50 Ω to Z_{opt} and hence reduces the loss at the output port [50]. This leads to a high transmitted power as well as a high power gain. Consequently, for the same gain level, the standard stacked PA necessities fewer nonlinear gain stages compared to a common-source (CS)-based PA and has the advantage of higher compression points. On the other hand, the cascode PA offers higher power gain than the standard stacked PA [51]. However, the cascode PA suffers from long-term reliability issues due to the excess swing, which is not an issue for the standard stacked PA. This is because the output impedance of the standard stacked PA is reduced by using small gate-to-ground capacitors, which contributes to making the drain–source amplitude of each stacked transistor equivalent for avoiding an excessive swing. However, in this design, the high gate bias will lead to an early compression, and meanwhile, the wideband matching will lessen the peak performance. Hence, the output swing of the standard stacked PA keeps a relatively low value, and there is still sufficient room under breakdown threshold to improve output swing and further enhance gain for a higher output power.

In order to further improve the output swing and enhance power gain, a pseudo triple-stacked PA under a 3-V power supply is introduced by intentionally increasing gate-to-ground

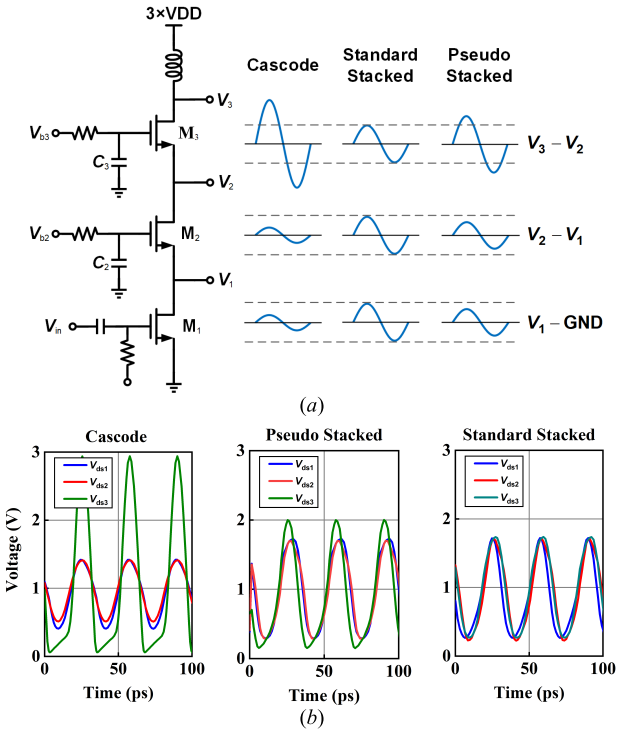


Fig. 15. Typical triple-stacked amplifier under a 3 × VDD supply. (a) Basic circuit structure. (b) Simulated transient V_{ds} of the three types of PA (P_{in} = 0 dBm), i.e., cascode, standard stacked, and pseudo stacked.

capacitors. A relatively high gate bias voltage (V_{GS1} = 650 mV) is chosen for compensating the loss from passive modules in the phased array and improving $P_{1\text{ dB}}$. The pseudo-stacked PA could be derived from the standard stacked PA. For a triple-stacked structure under 3 × VDD with the same transistor size as shown in Fig. 15(a), then there are $C_{\text{gs1}} = C_{\text{gs2}} = C_{\text{gs3}} = C_{\text{gs}}$ and $g_{m1} = g_{m2} = g_{m3} = g_m$. Driven by V_{in}, the output amplitude of each stage is expressed as follows:

$$\begin{cases} V_1 = V_{\text{in}} \cdot \dfrac{C_2 + C_{\text{gs}}}{C_2} \\ V_2 = V_{\text{in}} \cdot \dfrac{C_3 + C_{\text{gs}}}{C_3} \\ V_3 \approx V_{\text{in}} \cdot k \cdot g_m^2 \left(\dfrac{C_3}{C_3 + C_{\text{gs}}} R_{o2} r_{o3} \right) \end{cases} \tag{13}$$

where k is a power partition coefficient, R_{o2} is the equivalent output resistance of the second stage, and r_{o3} is the inherent output resistance. For a standard stacked structure, $V_1{:}V_2{:}V_3$ = 1:2:3 and $V_{\text{ds1,2,3}}$ is less than VDD, even with a relatively large margin for bulk CMOS. Assuming that output amplitudes are V_1', V_2', V_3', for pseudo-stacked state with the gate capacitors C_1', C_2', C_3', it is supposed to make V_{ds3}' ($= V_3' - V_2'$) close to VDD. Because $k \cdot g_m^2 R_{o2} r_{o2} \gg 1$, the change of the amplitude $V_3' - V_3 \gg V_2' - V_2$. V_{ds3} is expressed as

$$\begin{aligned} V_{\text{ds3}}' &= V_3' - V_2' = (V_3' - V_3) + V_3 - V_2 + (V_2' - V_2) \\ &\approx (V_3' - V_3) + V_3 - V_2 = V_3' - V_2 \end{aligned} \tag{14}$$

and V_3' is expressed as

$$V_3' \approx V_{\text{ds3}}' + V_2 = \text{VDD} + V_2. \tag{15}$$

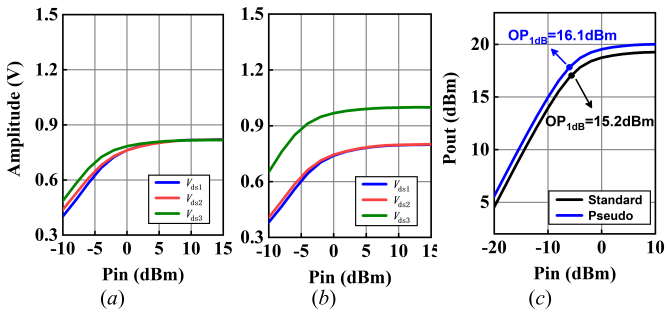


Fig. 16. Simulated results of the standard stacked PA and the pseudo-stacked PA. (a) Output amplitudes of the standard stacked PA. (b) Output amplitudes of the pseudo-stacked PA. (c) Comparison of P_{out} versus P_{in} curves.

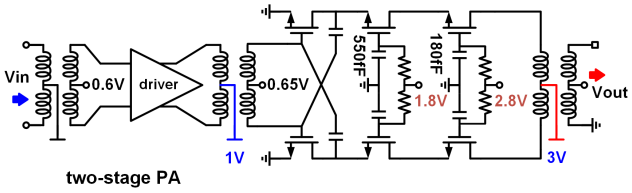


Fig. 17. Proposed PA with a triple-stacked output stage.

The relation between the modified capacitor C_3' and C_3 is obtained as

$$\frac{V_3'}{V_3} = \frac{C_3'/(C_3'+C_{\text{gs}})}{C_3/(C_3+C_{\text{gs}})} = \frac{\text{VDD}+2V_{\text{ds}}}{3V_{\text{ds}}} = \frac{2}{3}+\frac{1}{3}\frac{\text{VDD}}{V_{\text{ds}}}. \tag{16}$$

V_2' is reduced after C_3' increased. For averaging $V_{\text{ds1,2}}'$, C_2 should also be increasing moderately to C_2'. According to (13), C_2' is addressed as

$$C_2' = \frac{2C_{\text{gs}}\cdot C_3'}{C_{\text{gs}}-C_3'}. \tag{17}$$

Therefore, given a certain standard stacked amplifier, a pseudo-stacked PA could be obtained from (16) and (17). Fig. 16 shows the simulated output amplitude $V_{\text{ds1,2,3}}$ of the standard stacked PA and the pseudo-stacked PA (a transistor size of 300 μm/60 nm) against input power under different $C_{2,3}$ values. When $C_2 = 480$ fF and $C_3 = 110$ fF [see Fig. 16(a)], the stacked PA is with identical drain–source amplitude ($V_{\text{ds1,2,3}}$ is around 817 mV@10 dBm), and the corresponding equivalent C_{gs} is 205 fF. Using (16) and (17), it can be evaluated that C_2 is equal to 615 fF and C_3 is equal to 123 fF for the proposed stacked PA. Considering the large-signal compression, C_3 should be further increased here. In fact, C_2 of 570 fF and C_3 of 170 fF are adopted in this design, and the output amplitudes are shown in Fig. 16(b), where V_{ds3} is closer to VDD. Fig. 16(c) shows the simulated P_{out} versus P_{in} curves, which demonstrates that the proposed pseudo-stacked PA has higher power gain and $\text{OP}_{1\text{ dB}}$, compared to the standard one. In addition, Fig. 15(b) presents the transient V_{ds} in the nonlinear region of the three types of PA to indicate the difference among them in time domain.

The detailed schematic of the proposed two-stage PA is shown in Fig. 17. The pseudo-stacked structure under a 3.0-V supply is involved as the differential output stage for high P_{SAT} and $\text{OP}_{1\text{ dB}}$, driven by a CS input stage biased at 600 mV.

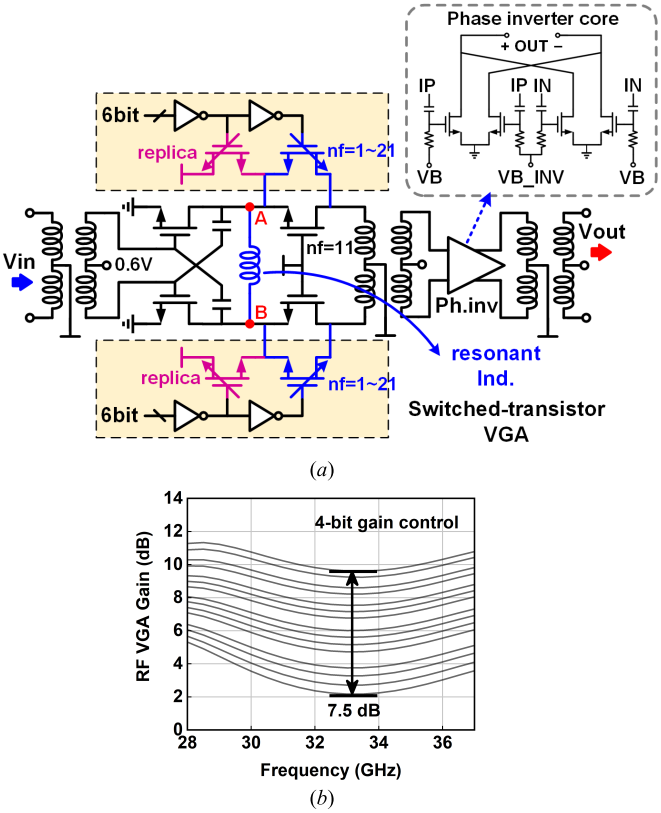


Fig. 18. Proposed 4-bit RF VGA with a phase inverter. (a) VGA schematic. (b) Simulated gain control of the VGA.

D. Other Building Blocks

The schematic of the current-mode RF VGA is shown in Fig. 18. The cascode input stage adopts the switched CG transistor technique: the effective current is regulated by changing the number of the CG finger, and then, the amplifier gain is changed. For restraining the additional phase shifting during gain control, replica CG-transistors are introduced. The ON–OFF state of the operation CG transistors is opposite to that of the corresponding replicas so that the parasitic capacitance C_p of nodes A and B between CS and CG will remain unchanged. Furthermore, a resonate inductor bridges nodes A and B for eliminating C_p. The VGA can provide 4-bit gain control in the range of 7.5 dB, with each step of 0.5 dB [as shown in Fig. 18(b)], and another 2-bit is used for fine calibration over process, voltage, and temperature (PVT) variation. The 6-bit control word corresponds to six sets of CG transistors, containing 21 fingers in total. The second gain stage of the VGA module is an active phase inverter, given in Fig. 18 (top right). Two CS differential pairs with cross-coupling structure achieve signal polarity switching. Unlike the widely used phase inverter like that in [33] that is cascode structure, the presented phase inverter removes the tail current source for high linearity and directly controls the gate bias by digital multiplexers to realize 180° phase shift.

In the RX link, power gain is severely attenuated through the passive blocks and the I/Q mixer, Thus, placing a buffer amplifier is necessary after the downconversion. The schematic

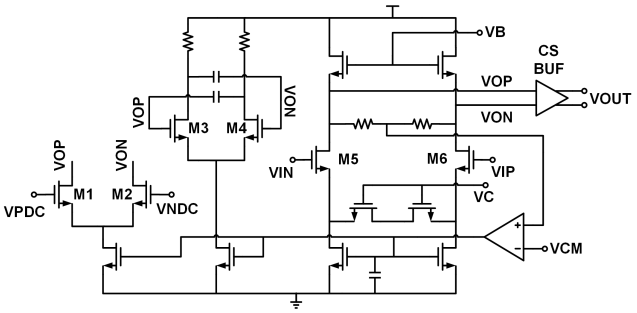


Fig. 19. RX BB buffer amplifier following the bimixer.

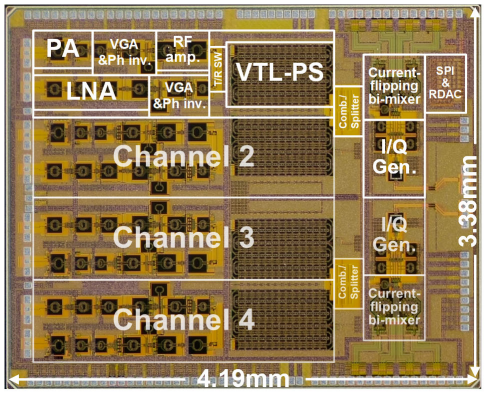


Fig. 20. Chip micrograph.

of the BB buffer with two gain stages is shown in Fig. 19. In the differential input stage, cross-couple C_C of $M_{3,4}$ provides negative capacitance to expand the bandwidth, and $M_{1,2}$ is used for the common-mode feedback. Afterward, a large-size output CS stage coupled to V_{op} and V_{on} is adopted to improve the RX output linearity.

IV. Measurement Results

The proposed *Ka*-band phased-array transceiver is fabricated in a standard 65-nm bulk CMOS process and occupies a die area of 4.19×3.38 mm^2. The chip micrograph is shown in Fig. 20. It can be seen that almost all silicon area is reused by radar and communication modes, including the dc, I/O, and ground-signal-ground (GSG) pads. The GSG pads are arranged at the left and right as the interfaces for RF signal and off-chip LO ($P_{LO} = 5$ dBm from a signal generator), respectively, and the baseband I/O pads are placed on the top and bottom sides. Several dc pads are also added at the left side to enhance the supplies of the two inner elements. The circuit performances for continuous-wave (CW) measurement are verified under a probe test, and the dual-function system validations are accomplished with full wire-bonding test. Except that the output stage of the PA is supplied under 3.0 V, all other building blocks in the transceiver are operated under 1.0 V. The PA is the most power-hungry block with 320-mW quiescent P_{dc} (240 mW for the output stage). In total, the TX mode consumes 422 mW per channel and the RX mode consumes 172 mW per channel.

A. CW Measurement

In the TX mode, the measured small-signal reflection coefficients at the baseband are shown in Fig. 21(a). Compared to the simulation, the measured TX baseband bandwidth is reduced to 3.5 GHz, which is caused by the bonding wires and PCB routing. Given that the baseband bandwidth is less than the RF bandwidth, the power gain is tested segmentally with different LO frequencies between 26 and 39 GHz (the same for the RX). As seen in Fig. 21(b), the peak power gain of 22.2 dB is measured with 3-dB bandwidth B_{TX} within 28.1–36.2 GHz, according to the envelope of the gain curves. As for the large-signal performance shown in Fig. 21(c), the $OP_{1\ dB}$ achieves a peak value of 17.4 dBm at 28 GHz and is above 12.2 dBm across the band B_{TX}. The measured in-band P_{SAT} is >17.0 dBm with the peak of 19.9 dBm at 28 GHz.

In the RX mode, the reflection coefficient of the baseband buffer output is given in Fig. 22(a), with a 1.5-GHz single sideband (SSB) bandwidth of < -10 dB, which also limits the baseband bandwidth for the RX mode to 3.5 GHz. As shown in Fig. 22(b), the RX power gain achieves the maximum value of 34.7 dB with a 3-dB bandwidth of 28.7–37.0 GHz. The measured minimum RX NF is 4.8 dB. The RX input linearity against frequency under maximum gain and minimum gain is shown in Fig. 22(c). The $IP_{1\ dB}$ is > -37.2 dBm under the maximum gain and > -31.5 dBm under the minimum gain. At the maximum gain state, the phase control is measured and plotted in Fig. 23. With 6-bit control words, a 160° phase range is covered at 30 GHz and the relative phase error of each step is less than ±5°. For the gain control capability, the measured gain control range is 7 dB tuned by 4-bit control words. The measured root-mean-square (rms) gain error against frequency is shown in Fig. 23 with a maximum value of 0.57 dB. The channel isolation is demonstrated by measuring the impact of phase control on an adjacent channel. The measured equivalent isolation of TX channels is better than −30.7 dB.

For a wideband zero-IF transceiver, the LO leakage will drop in the operation band, which leads to severe saturation distortion of the signal. To enhance the LOFT rejection, this design employs current-compensation-based LOFT calibration with 8-bit tuning in the I/Q mixer. There are two calibration current sources placed in each Gilbert quad to finely correct the differential-mode dc offset. Another concerned performance is image rejection ratio (IRR) determined by the I/Q orthogonality, for ensuring the communication quality and avoiding image interference. Therefore, the mixer and the PPF buffer are designed with tunable biases, and the switched resistors are hired in the PPF as well. In order to verify the LOFT rejection and IRR offered by the methods mentioned above, a single CW spectrum in the TX mode is measured and shown in Fig. 24. After calibration, the LOFT rejection is −50.5 dBc and the IRR is 43.4 dBc at 31 GHz.

B. Communication System Measurement

For wireless communication system measurements, the testing board prototype of the transceiver chip is enclosed in a metallic electrostatic shield, with the pluggable RF and BB interfaces. The test setup for the communication measurement is shown in Fig. 25. A TX-mode chip and an RX-mode chip are separated by 1 m and each of them is connected to a horn antenna. An arbitrary wave generator (AWG) is utilized to provide baseband 100-/400-MHz data flow in QAM.

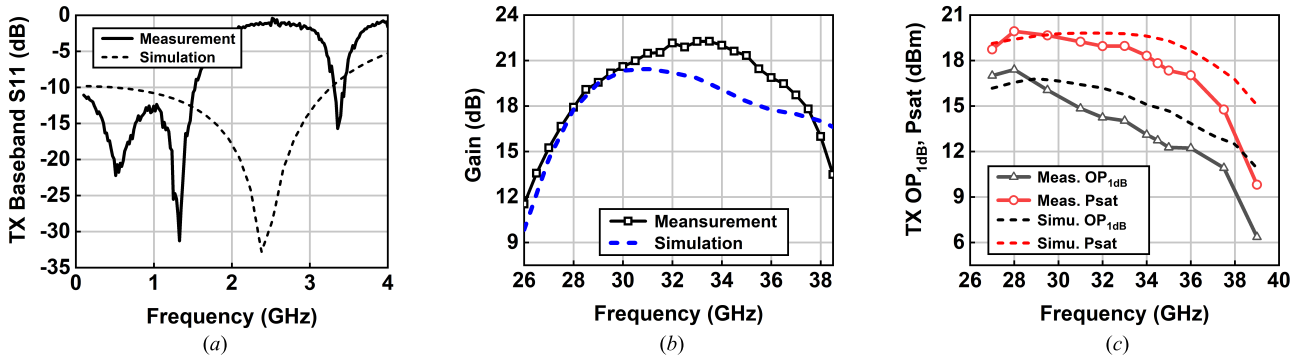


Fig. 21. Measured results of TX for CW measurement. (a) Baseband reflection of TX. (b) TX power gain. (c) Linearity performance of TX.

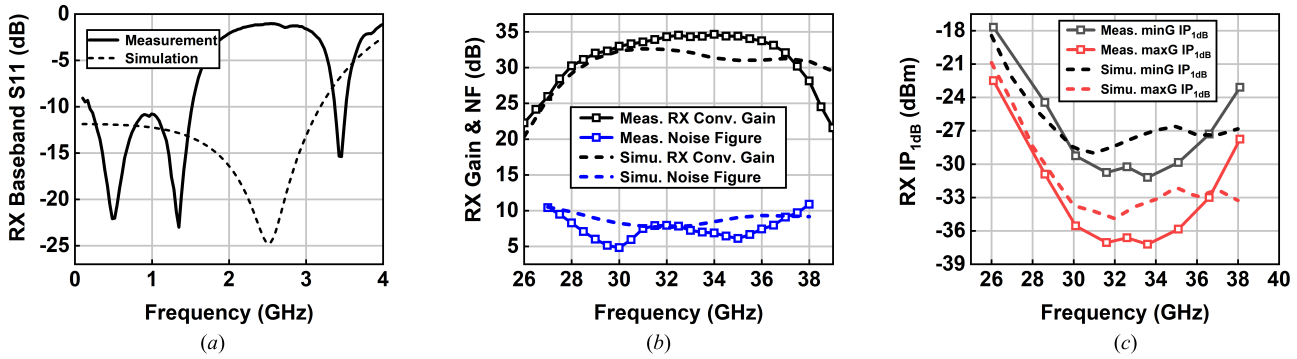


Fig. 22. Measured results of RX for CW measurement. (a) Baseband reflection of RX. (b) Power gain and NF of RX. (c) $IP_{1\ dB}$ of RX under max. and min. gain states.

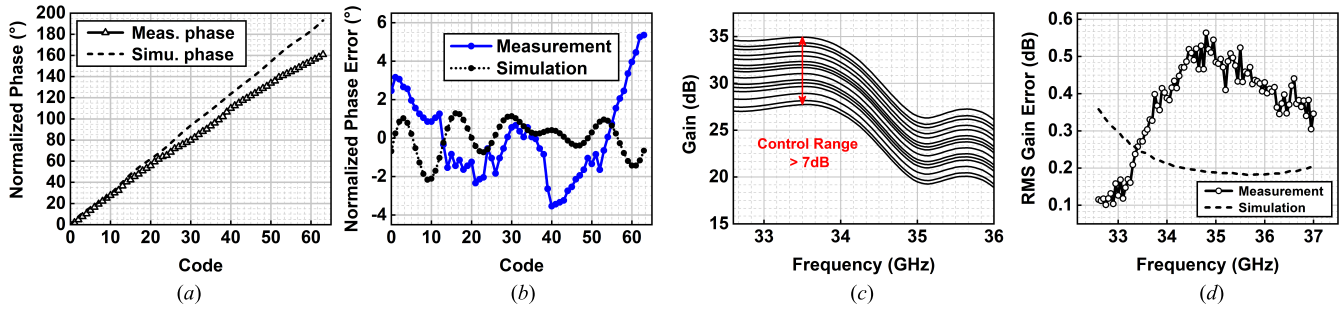
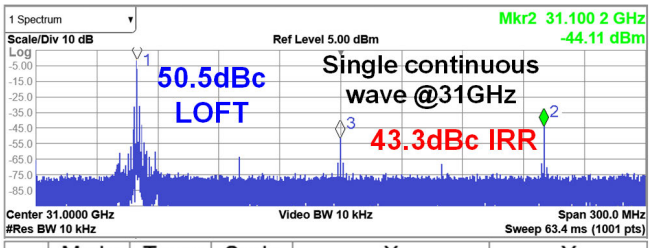


Fig. 23. Measured phase control and gain control results. (a) Normalized phase shifting. (b) Relative phase error versus control code. (c) Gain tuning curves with LO frequency @32.5 GHz. (d) RMS gain error with LO frequency @32.5 GHz.



	Mode	Trace	Scale	X	Y
1	N	1	f	30.899 8 GHz	-0.7755 dBm
2	N	1	f	31.100 2 GHz	-44.11 dBm
3	N	1	f	31.000 0 GHz	-51.38 dBm

Fig. 24. LOFT and IRR at 31-GHz LO with 10-MHz offset.

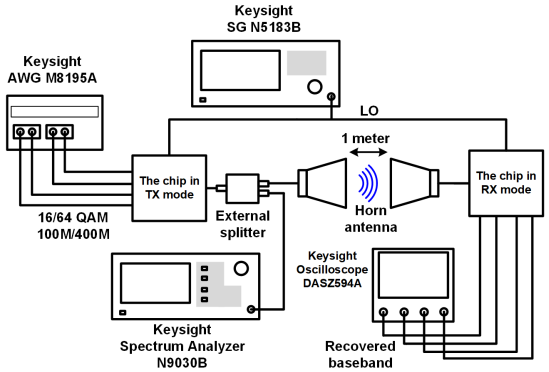
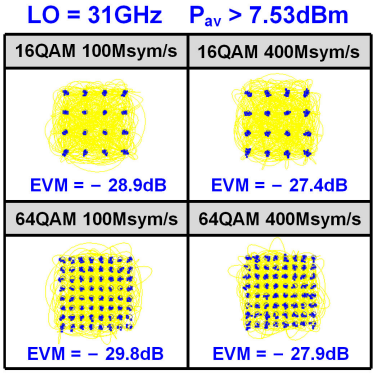
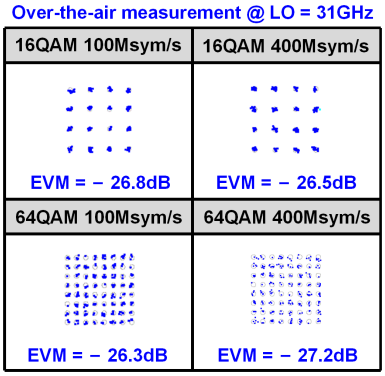


Fig. 25. Communication measurement setup.

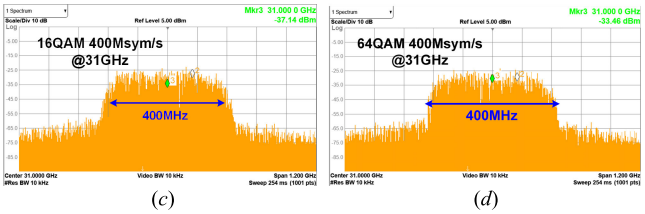
An oscilloscope is placed after the RX chip to process the RX baseband signal and analyze the communication quality. The off-chip LO is provided by a signal generator and distributed to the two chips by a power divider. At the TX output, another power divider is used to deliver the transmitted RF signal to a spectrum analyzer so that the signal can be convenient for observation. As shown in Fig. 26, the measured



(a)



(b)



(c) (d)

Fig. 26. Communication measurement results. (a) TX EVM under 16/64 QAM. (b) OTA EVM under 16/64 QAM. (c) 16 QAM modulated signal spectrum. (d) 64 QAM modulated signal spectrum.

TX EVM in single carrier mode are −28.9, −27.4, −29.8, and −27.9 dB under 100-Msym/s 16-QAM, 400-Msym/s 16-QAM, 100-Msym/s 64-QAM, and 400-Msym/s 64-QAM, respectively. The transceiver achieves the OTA TX-to-RX EVM of −26.8, −26.5, −26.3, and −27.2 dB under 100-Msym/s 16-QAM, 400-Msym/s 16-QAM, 100-Msym/s 64-QAM, and 400-Msym/s 64-QAM, respectively. With these modulation test cases, the measured adjacent channel leakage ratio is lower than −30 dBc.

C. Radar System Measurement

The radar system function is measured in a microwave anechoic chamber, with corner reflectors used as the detecting targets. The radar measurement setup is shown in Fig. 27. An FPGA-based processor with inherent A/D converters is employed to generate the baseband pulsed chirp signal by digital direct synthesis. The orthogonalization of the signal is conducted by an external quadrature coupler. Two chips with horn antenna connected operate in the TX mode and RX mode, and the baseband echo signal is sent to the processor to calculate the sensing results.

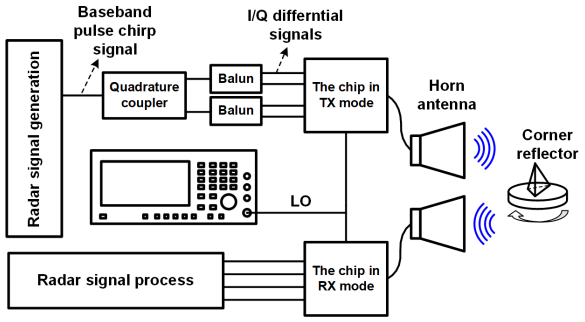


Fig. 27. Radar measurement setup.

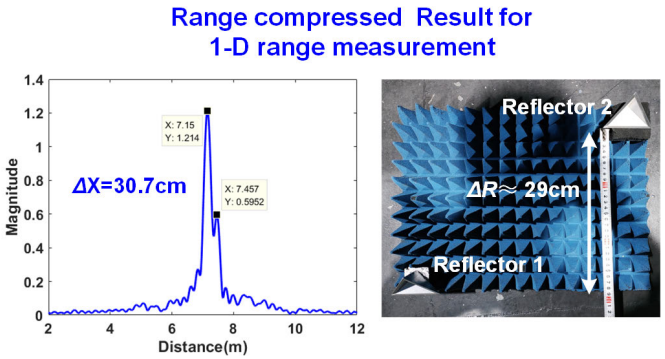


Fig. 28. Scene photograph and response waveform of 1-D range measurement.

In the 1-D measurement, the baseband chirp frequency varies from 100 to 900 MHz. The measured minimum detection range of 22 cm is obtained in the 1-D measurement. Fig. 28 shows the accuracy of the relative range measurement. For an actual range of 29 cm, the corresponding range compressed result implies that the measured relative distance is 30.7 cm. In the 2-D measurement, the ISAR technique is used. The reflectors are placed on a revolving stage surrounded by wave absorbing material, which rotates along the azimuth direction with an angular speed of 1°/s. The baseband pulsed chirp waveform has a frequency range from 550 to 1050 MHz, which is limited by the external quadrature coupler. When the reflectors rotate, the detecting sequence containing 2048 pulses modulates a 31-GHz LO and is emitted continuously, with a PRF of 1000 Hz. According to (12), the azimuth resolution is 13.54 cm. Finally, the measured result of the relative 2-D position is (43.7, 23.7 cm), corresponding to the actual value (45, 24 cm), as shown in Fig. 29.

Table I summarizes the performance summary of the proposed transceiver and comparison with the state-of-the-art phased-array designs at *K*- and *Ka*-bands. As previously mentioned, most phased-array TX/RX circuits are solely targeted for either communication or radar system, and hence, the cited publications listed in the table mainly includes several communication transceivers [24], [26], [27], [28], [52]. Mannem et al. [38] presented a dual-functional phased-array transmitter with frequency modulated array scheme, and it is mainly used for angular measures with narrow RF and BB bands as mentioned in Section I. Pei et al. [53] also presented a dual-band communication/radar transmitter, with both high output power

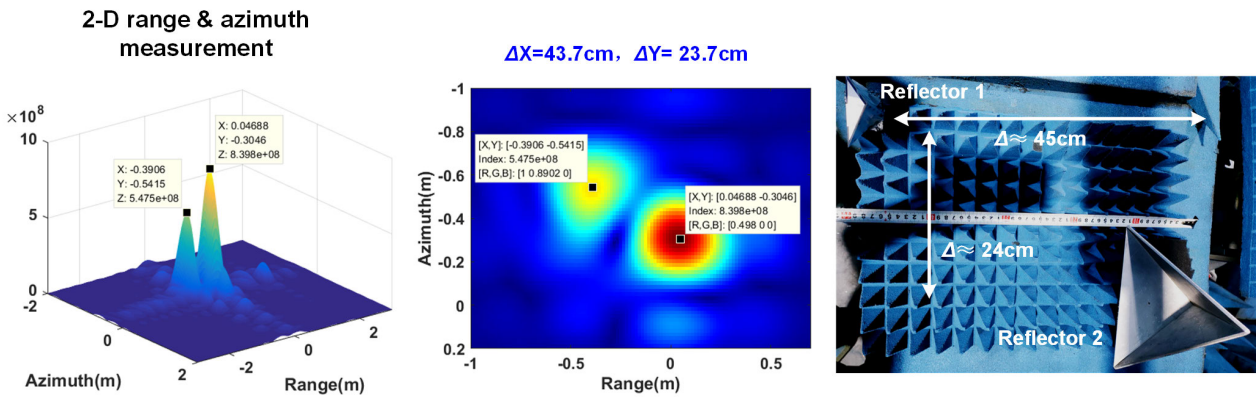


Fig. 29. Two-dimensional range and azimuth sensing measurement. (a) Stereo-image of 2-D measurement. (b) Plane image of 2-D measurement. (c) Picture of the reflectors in 2-D measurement.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[38] JSSC2022	[28] ISSCC2022	[26] ISSCC2020	[24] JSSC2018	[27] ISSCC2018	[52] TMTT2021	[53] JSSC2015
Technology	65nm CMOS	45nm CMOS SOI	28nm CMOS SOI	28nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	0.25 μm BiCMOS
Mode	**COMM./ Pulse Radar**	**COMM./ FMA Radar** (TX Only)	COMM.	COMM.	COMM.	COMM.	COMM.	**COMM./ Radar** (TX Only)
RF Band (GHz)	28.7-36.2	29-31	26/28/39	25-30.5	25.8-28.0	25-30.5	37.5-39.5	29.5-35
Channels	4 Ch.	4 Ch.	16 Ch.	16 Ch.	8 Ch.	24 Ch.	8TX/4RX	1Ch.
TX Gain (dB)	22.2	26	-	30-60	48	34-44	32.3	>25
TX Psat/Ch. (dBm)	**19.9**	18	-	>16.5	9.5	>14	-	>14.5
TX OP_{-1dB}/Ch. (dBm)	**17.4**	-	-	-	-	>12	10.8	>11.4
RX Gain (dB)	34.7	NA	-	16-59	30-69	32-34	39	NA
RX NFmin (dB)	4.8	NA	4.3	4.2	6.7@Ghigh 13.7@Glow	4.4	6.8	NA
RX IP_{-1dB}/Ch.(dBm)	>−37.2	NA	-	-	−68.9@Ghigh −34.8@Glow	-	−40	NA
OTA EVM (dB)	−26.5 16QAM 1.6Gb/s −27.2 64QAM 2.4Gb/s	−25dB (TX) 64QAM 3.0Gb/s	−27.1 (TX) 77Mb/s −26.1 (RX) 4200Mb/s	−32.5 (TX) 64QAM 4.8Gb/s −33.1 (TX) 64QAM 4.8Gb/s	<−28 64QAM LTE 120Mb/s	<−25dB (RX) 64QAM 2.4Gb/s	−30.3 64QAM 2.4Gb/s −34.38 256QAM 1.6Gb/s	−29.6 64QAM
Power (mW)	594/Ch.	-	307/Ch.	144/Ch.	135/1 Ch.	132/Ch.	187/Ch. (TX) 172/Ch. (RX)	732
Chip Area (mm^2)	14.16	14.85	25.08	30.0	7.28	27.76	-	2.85
Range Resolution (m)	0.22	NA	NA	NA	NA	NA	NA	NA
Azimuth Resolution	0.14m	<2°	NA	NA	NA	NA	NA	NA

and high linearity considered. Nevertheless, there are few discussions on the radar measurement, the radar scheme, and the sensing resolution. To some extent, the proposed work is meaningful that it is an attempt to accomplish and demonstrate a joint design for radar/communication with both the uplink and downlink. In terms of circuit performance compared to other designs in the table, the proposed transceiver shows a wide RF bandwidth, decent power gain, NF, and RX $P_{1\ dB}$. In addition, this work features a high TX $P_{1\ dB}$ of 17.4 dBm for the communication mode and a decent P_{SAT} of 19.9 dBm for the radar mode.

V. CONCLUSION

A four-channel *Ka*-band phased-array transceiver chip for radar sensing and wireless communication is presented in this article. Fabricated in 65-nm CMOS process, this transceiver adopts a direct conversion architecture so that the building blocks are fully reused by the radar and communication modes. The methods, such as current-flipping active bidirectional mixer, true-time-delay TL-PS, pseudo-stacked PA, and wideband baseband buffer, are introduced to cater for the requirements on dual-function co-design. With 6-bit phase control and 4-bit gain control, the proposed transceiver covers 7.5-GHz RF bandwidth and realizes 22.2-/34.7-dB peak gain of the TX/RX modes. The measured peak TX $OP_{1\ dB}$ of 17.4 dBm and the minimum NF of 4.8 dB are achieved. The wireless measurements demonstrate that the proposed transceiver is able to feature dual function and is competent for centimeter-level 1-D/2-D radar sensing and 64-QAM OTA wireless link.

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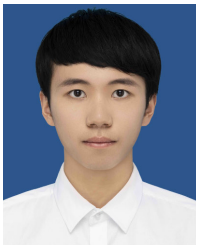

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